IN THE CLAIMS

Claim 1 (original): A method for programming a memory device having a programming node, comprising:

providing a programming voltage to the programming node;

using the programming voltage to generate a load current;

generating a load voltage at a compensation node of the memory device;

generating an error voltage in response to the load voltage; and

changing the load current in response to the error voltage.

Claim 2 (original): The method of claim 1, wherein generating the error voltage includes comparing a reference voltage with the load voltage.

Claim 3 (original): The method of claim 2, wherein the error voltage increases the load current when the reference voltage has a greater value than the load voltage.

Claim 4 (original): The method of claim 1, wherein changing the load current further includes providing an enable signal at a switching terminal.

Claim 5 (original): The method of claim 1, wherein providing the programming voltage includes providing the programming voltage to a plurality of programming nodes.

Claim 6 (original): The method of claim 5, wherein providing the programming voltage includes providing the programming voltage to sixteen programming nodes.

Claim 7 (original): The method of claim 1, wherein changing the load current includes increasing the load current.

Claim 8 (original): A method for regulating a programming voltage in a memory device, comprising:

generating a load current in accordance with the programming voltage; and

changing the load current in response to a programming load by applying the programming voltage to a load compensation network, wherein the load compensation network changes the load current to simulate programming a predetermined number of data bits of the memory device.

Claim 9 (original): The method of claim 8, wherein generating the load current further includes generating a load current in accordance with the number of data bits being programmed.

Claim 10 (original): The method of claim 9, wherein the number of data bits being programmed is sixteen.

Claim 11 (original): The method of claim 8, wherein the predetermined number of data bits is sixteen.

Claim 12 (original): The method of claim 8, wherein changing the load current includes generating a load compensation current through a programming load.

Claim 13 (original): The method of claim 8, wherein changing the load current includes:

comparing a compensation voltage signal with a reference voltage signal to generate an error voltage signal;

generating an output voltage signal in accordance with the error voltage signal; and

using the output voltage signal to change the load current.

Claim 14 (original): The method of claim 13, wherein using the output voltage signal to change the load current includes activating a transistor.

Claims 15-21 (canceled)